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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,173	GAT ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/31/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending.

2. The office acknowledges the following papers:

Patent application filed on 12/31/2003.

Priority

3. No claim for priority has been made in this application.

Drawings

4. The Examiner contends that the drawings submitted on 12/31/2003 are acceptable for examination proceedings.

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 5 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 has the limitation "in two cycles, storing said prediction for two sequential lines in said queue and delivering said prediction to said instruction fetch unit." It's unclear if one prediction or two predictions are stored in the queue and if one or two predictions are delivered to the instruction fetch unit. The specification supports storing two branch predictions in the queue in two cycles and sending one prediction to the instruction fetch unit (Figures 1 and 3). For examination purposes, the limitation will be interpreted as "in two cycles, storing branch [[said]] predictions for two sequential lines in said queue and delivering [[said]] a single branch prediction to said instruction fetch unit."

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1, 7-9, 12, 17, and 20 are rejected under 35 U.S.C. §102(b) as being anticipated by Reinman et al. ("Optimizations Enabled by a Decoupled Front-End Architecture").

12. As per claim 1:

Reinman disclosed a method comprising:

Storing a branch prediction in a queue (Reinman: Figure 5, sections 4.1 and 5.2)(Predictions are stored in the fetch target queue); and

Delivering said stored branch prediction to an instruction fetch unit (Reinman: Figure 5, section 4.1).

13. As per claim 7:

Reinman disclosed the method as in claim 1, comprising generating during a cycle a prediction for a line, said line being other than the line being fetched by said instruction fetch unit during said cycle (Reinman: Figure 5, section 4.1)(Figure 5 shows branch predictions being generated and stored in the instruction fetch queue. Thus, the predictor deals with different instructions than the instruction fetch unit during the same cycle.).

14. As per claim 8:

Claim 8 essentially recites the same limitations of claim 7. Therefore, claim 8 is rejected for the same reasons as claim 7.

15. As per claim 9:

Claim 9 essentially recites the same limitations of claim 17. Claim 9 additionally recites the following limitations:

A branch prediction unit (Reinman: Figure 5, section 4.1); and

An instruction fetch unit (Reinman: Figure 5, section 4.1).

16. As per claim 12:

Claim 12 essentially recites the same limitations of claim 1. Claim 12 additionally recites the following limitations:

A branch prediction unit (Reinman: Figure 5, section 4.1); and

An instruction fetch unit (Reinman: Figure 5, section 4.1).

17. As per claim 17:

Reinman disclosed a method comprising:

Generating during a cycle, in a branch prediction unit of a processor, a branch prediction for a first line (Reinman: Figure 5, sections 4.1 and 5.2); and

Fetching during said cycle, in an instruction fetch unit of said processor, an instruction for a second line (Reinman: Figure 5, section 4.1).

18. As per claim 20:

Claim 20 essentially recites the same limitations of claim 12. Claim 20 additionally recites the following limitations:

DRAM (Reinman: Figure 5)(Figure 5 shows a prefetch unit that fetches instructions from L2 cache or higher memories, such as main memory. Official notice is taken that the L2 cache or higher memory like main memory could either comprise a DRAM.).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2, 5-6, 10, and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Reinman et al. ("Optimizations Enabled by a Decoupled Front-End Architecture").

21. As per claim 2:

Reinman disclosed the method as in claim 1.

Reinman failed to teach generating said branch prediction for two sequential lines in two clock cycles.

However, it would have been obvious to one of ordinary skill in the art that if two branch instructions occurred in sequential order, that the branch predictor would have made two predictions in a row. It would have also been obvious to one of ordinary skill in the art that a branch predictor could take a single cycle to generate a branch prediction. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that two sequential branch predictions could have been generated in two clock cycles.

22. As per claim 5:

Reinman disclosed the method as in claim 1.

Reinman failed to teach in two cycles, storing branch predictions for two sequential lines in said queue and delivering a single branch prediction to said instruction fetch unit.

However, it would have been obvious to one of ordinary skill in the art that if two branch instructions occurred in sequential order, that the branch predictor would have

made two predictions in a row. It would have also been obvious to one of ordinary skill in the art that a branch predictor could take a single cycle to generate a branch prediction. It would have also been obvious to one of ordinary skill in the art that if the instruction fetch queue was empty, then a single prediction would be delivered to the instruction fetch unit in the two cycle period. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that two predictions could be stored in the instruction fetch queue and one of the predictions could be delivered to the instruction fetch unit.

23. As per claim 6:

Reinman disclosed the method as in claim 1.

Reinman failed to teach generating branch predictions for a stream of addresses during a stall of said instruction fetch unit.

However, it would have been obvious to one of ordinary skill in the art that the only time it would have been necessary for the branch predictor to stop generating predictions is when the instruction fetch queue is full. It would have also been obvious to one of ordinary skill in the art that the instruction fetch unit could be stalled on an instruction cache miss while the instruction fetch queue was not full. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the predictor could continue predicting branches while the instruction fetch queue was stalled as long as the instruction fetch queue was not full.

24. As per claim 10:

Reinman disclosed the processor as in claim 9, wherein said branch prediction unit comprises a queue configured to store branch predictions (Reinman: Figure 5, sections 4.1 and 5.2)(It would have been obvious to one of ordinary skill in the art at the time of the invention that the FTQ could have been placed within the branch prediction unit. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

25. As per claim 18:

Reinman disclosed a method as in claim 17, comprising storing said branch prediction in a data storage area of said branch prediction unit (Reinman: Figure 5, sections 4.1 and 5.2)(It would have been obvious to one of ordinary skill in the art at the time of the invention that the FTQ could have been placed within the branch prediction unit. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

26. Claims 3-4, 13-14, 19, and 21-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Reinman et al. ("Optimizations Enabled by a Decoupled Front-End Architecture"), further in view of Stiles et al. (U.S. 5,515,518).

27. As per claim 3:

Reinman disclosed the method as in claim 1.

Reinman failed to teach segmenting a cache of a branch predictor into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses

having odd-numbered indexes.

However, Stiles disclosed segmenting a cache of a branch predictor into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes (Stiles: Figure 9 element 155, column 15 lines 51-58)(Stiles disclosed a direct-mapped branch prediction cache. The segmented cache as claimed is a direct-mapped branch prediction cache that is divided into a lower and upper segment that divides odd and even instruction addresses. It would have been obvious to one of ordinary skill in the art at the time of the invention that having a segmented cache has no effect on the accuracy of the branch prediction and is simply slightly reorganizing the layout of the cache. Also, it would have been obvious to one of ordinary skill in the art at the time of the invention that the segmented cache would have no effect on the access time of the prediction entries. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the segmented cache. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

The advantage of a direct mapped cache is that there are more entries that can be used compared to a set-associated or fully associative cache of the same size (Stiles: Column 3 lines 64-67 continued to column 4 lines 1-10). Another advantage is that the access time of the direct mapped cache is decreased because of the assumption that the tag and look-up addresses match (Stiles: Column 4 lines 20-28). Direct-mapped caches are also cheaper to use than their set or fully associative

counterparts due to fewer comparators needed to check for correct tags. The advantages of increased capacity, decreased costs, and decreased access latency would have motivated one of ordinary skill in the art at the time of the invention to implement a direct-mapped branch prediction cache. Thus, it would have been obvious to implement a direct-mapped branch prediction cache into the processor of Reinman for the advantages of increased capacity, decreased costs, and decreased access latency.

28. As per claim 4:

The method as in claim 3, wherein an index of one of two sequential lines corresponds to an entry on said first side of said cache, and an index of another of said two sequential lines corresponds to an entry on said second side of said cache (Stiles: Figure 9 element 155, column 15 lines 51-58)(It's inherent that in the segmented cache two sequential instructions with an odd instruction address and an even instruction address would be located in different segments of the cache.).

29. As per claim 13:

Claim 13 essentially recites the same limitations of claim 3. Therefore, claim 13 is rejected for the same reasons as claim 3.

30. As per claim 14:

Claim 14 essentially recites the same limitations of claim 4. Therefore, claim 14 is rejected for the same reasons as claim 4.

31. As per claim 19:

Claim 19 essentially recites the same limitations of claim 3. Therefore, claim 19 is rejected for the same reasons as claim 3.

32. As per claim 21:

Claim 21 essentially recites the same limitations of claim 3. Therefore, claim 21 is rejected for the same reasons as claim 3.

33. As per claim 22:

Claim 22 essentially recites the same limitations of claim 3. Therefore, claim 22 is rejected for the same reasons as claim 3.

34. Claims 9, 11-12, and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Totsuka et al. (U.S. 6,640,298), further in view of Parady (U.S. 6,907,520).

35. As per claim 9:

Totsuka and Parady disclosed a processor comprising:

A branch prediction unit (Totsuka: Figure 7); and

An instruction fetch unit (Parady: Figure 1 element 102), wherein said branch prediction unit is to, in a prediction period, generate a prediction on a first line (Parady: Figure 1 element 120), and said instruction fetch unit is to in said prediction period, fetch instructions for a second line (Parady: Figure 1 element 102).

Totsuka disclosed a hybrid branch prediction unit that can select amongst a plurality of branch predictions. The advantage of using a hybrid predictor is that it allows for branches that alternate between taken and not taken to be correctly predicted

(Totsuka: Column 2 lines 6-28). The ability to correctly predict branch instruction more often would have motivated one of ordinary skill in the art to implement the hybrid predictor of Totsuka in the processor of Parady. Thus, it would have been obvious to one of ordinary skill in the art to use the branch prediction scheme of Totsuka in the processor of Parady for the advantage of increased branch prediction accuracy.

36. As per claim 11:

Totsuka and Parady disclosed the processor as in claim 9, wherein said branch prediction unit is to deliver a branch prediction to said instruction fetch unit in the same prediction period as said branch prediction unit writes said branch prediction to a queue (Totsuka: Figure 7 element 804, column 5 lines 42-46)(In figure 7, the branch prediction is sent to the queue and sent out of the branch predictor at the same time. Thus, it would have been obvious to one of ordinary skill in the art that the combination of Totsuka and Parady would have resulted in the prediction being sent to the instruction fetch unit at the same time it's sent to the queue.).

37. As per claim 12:

Totsuka and Parady disclosed a processor comprising;

An instruction fetch unit (Parady: Figure 1 element 102); and

A branch prediction unit (Totsuka: Figure 7), said branch prediction unit comprising a queue to store branch predictions (Totsuka: Figure 7 elements 806 and 807, column 5 lines 62-67), and said branch prediction unit to deliver branch predictions stored in said queue to said instruction fetch unit (Totsuka: Figure 7 element 804, column 5 lines 42-46)(In figure 7, the branch prediction is sent to the queue and sent

out of the branch predictor at the same time. Thus, it would have been obvious to one of ordinary skill in the art that the combination of Totsuka and Parady would have resulted in the prediction being sent to the instruction fetch unit at the same time it's sent to the queue.).

Totsuka disclosed a hybrid branch prediction unit that can select amongst a plurality of branch predictions. The advantage of using a hybrid predictor is that it allows for branches that alternate between taken and not taken to be correctly predicted (Totsuka: Column 2 lines 6-28). The ability to correctly predict branch instruction more often would have motivated one of ordinary skill in the art to implement the hybrid predictor of Totsuka in the processor of Parady. Thus, it would have been obvious to one of ordinary skill in the art to use the branch prediction scheme of Totsuka in the processor of Parady for the advantage of increased branch prediction accuracy.

38. As per claim 16:

Claim 16 essentially recites the same limitations of claim 11. Therefore, claim 16 is rejected for the same reasons as claim 11.

39. Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Reinman et al. ("Optimizations Enabled by a Decoupled Front-End Architecture"), further in view of Giacalone et al. (U.S. 6,272,624).

40. As per claim 15:

Reinman disclosed the processor as in claim 12.

Reinman failed to teach wherein said branch prediction unit is to look up two lines in a prediction period.

However, Giacalone disclosed wherein said branch prediction unit is to look up two lines in a prediction period (Giacalone: Figure 3, column 8 lines 47-67 continued to column 9 lines 1-34)(A line is a single instruction. Figure 3 shows multiple branch instructions being predicted within a single prediction period.).

The advantage of using a branch predictor that can predict multiple branch instructions per cycle is that it's needed to achieve high performance in very wide superscalar processors (Giacalone: Column 2 lines 26-34). One of ordinary skill in the art would have been motivated by increased performance in superscalar processors to add the branch predictor of Giacalone to the processor Reinman. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the branch predictor of Giacalone to the processor of Reinman for the advantage of increased performance in a superscalar processor.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jain et al. (U.S. 5,809,320), taught a branch queue storing branch predictions.

Sinharoy (U.S. 6,877,089), taught a branch information queue that stored branch predictions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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